

**AMENDMENT AND RESPONSE UNDER 37 CFR § 1.111**

Serial Number: 10/829,559

Filing Date: April 22, 2004

**Title: METHOD AND APPARATUS FOR IMPLEMENTING A MULTIPLIER UTILIZING DIGITAL SIGNAL PROCESSOR BLOCK MEMORY EXTENSION**

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**REMARKS**

Applicants respectfully request the Examiner's reconsideration of the present application as amended.

Claims 1-20 are pending in the present application.

The drawings are objected to under 37 CFR 1.83(a).

Claims 1-20 are rejected under 35 U.S.C. §101, because the claimed invention is deemed to be directed to non-statutory subject matter.

Claims 1-4, 6-7, 9, 11-20 are rejected under 35 U.S.C. §102(e) as being unpatentable over U.S. Patent no. 6,907,024 ("Regis").

Claim 5 is rejected under 35 U.S.C §103(a) as being unpatentable over Regis.

No art rejections were issued by the Office to claims 8 and 10 by the Office.

Claims 2 and 4 have been canceled.

Claims 21 and 22 have been added.

Claims 1, 11, and 17 have been amended.

Support for new claims 21 and 22, and amended claims 1, 11, and 17 is found at paragraphs [0003], and [0040]-[0053] of the specification, Figures 5-10 of the drawings, and claims 1-20 as originally filed. No new matter has been added.

The drawings are objected to under 37 CFR 1.83(a). The Office Action mailed 9/10/2007 states in part that

The drawings must show every feature of the invention specified in the claims. Therefore, the limitations/features cited in claims 1 and 7-9 must be shown or the feature(s) canceled from the claim(s).

(9/10/2007 Office Action, p. 2).

Applicants submit that the drawings show the feature of the invention specified in claims 1, 7, and 9. For example, Applicants refer the Office to block 510, 530, and 540 of Figure 5, and

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701-704, and 710 of Figure 7. Paragraph [0040] describes block 510 as a DSP block that is configured to support 9\*9 bit multiplication and that multiplies the 9 most significant bits of a first number with the 9 most significant bits of a second number (generating a product by multiplying). Block 530 of Figure 5 is a memory block configured to store values the represent all the combinations of multiplying the 3 least significant bits of the first number with the 5 most significant bits of the second number (retrieving a stored value designated as a product).

Paragraph [0049] describes that the output from block 510 is scaled 4 bits to the left (4L) and that the output from block 530 is scaled 5 bits to the left (5L) (scaling the product). The scaling is described as being achieved by routing the outputs on routing resources 701-704 to adder 710 (summing the scaled product).

Additional examples are provided in Figures 6, and 8-10 and described in paragraphs [0041], and [0050]-[0054]. Furthermore, the specification points out that other multiplier bit maps may be generated using the techniques described and that a different allocation of resources on the FPGA may be made to designated bits in the numbers to be multiplied, and that other multipliers may be configured.

Applicants submit that in view of the above explanation, the drawings satisfy the requirements under 37 CFR 1.83(a).

Claims 1-20 are rejected under 35 U.S.C. §101. The Office Action mailed 9/10/2007 states in part that

Claims 1-20 cite a method and device for sum shift products in accordance with a mathematical algorithm. In order for claims to be statutory, claims must either include a practical/physical application or a concrete, useful, and tangible result. However, claims 1-20 merely disclose steps/components for sum shift products without further disclosing a practical/physical application or a useful and tangible result since the claims appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular

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practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein.

(9/10/2007 Office Action, p. 3).

This rejection is respectfully traversed for the following reasons.

Applicants submit that Claims 1, 3, and 5-20 cover a practical application of a judicial exception. As noted in the M.P.E.P.,

A claimed invention is directed to a practical application of a 35 U.S.C. §101 judicial exception when it:

- (A) "transforms" an article or physical object to a different state or thing; or  
(B) otherwise produces a useful, concrete and tangible result, based on the factors discussed below.

(M.P.E.P. § 2106(IV)(C)(2))(emphasis added).

According to M.P.E.P. § 2106(IV)(C)(2)(1), the inquiry into whether a claim covers a practical application of a 35 U.S.C. 101 judicial exception begins with a threshold determination.

M.P.E.P. § 2106(IV)(C)(2)(1) states:

USPTO personnel first shall review the claim and determine if it provides a transformation or reduction of an article to a different state or thing. If USPTO personnel find such a transformation or reduction, USPTO personnel shall end the inquiry and find that the claim meets the statutory requirement of 35 U.S.C. 101. If USPTO personnel do not find such a transformation or reduction, they must determine whether the claimed invention produces a useful, concrete, and tangible result.

**Claims 1, 3, and 5-10 Transform an Article to a Different State**

Applicants submit that the method of Claim 1 transforms and reduces articles to a different state or thing. Claim 1 recites a method for performing multiplication on a field programmable gate array. The method includes generating a product by multiplying a first plurality of bits from a first number and a first plurality of bits from a second number using a digital signal processor (DSP) configured to perform multiplication on a fewer number of bits

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than those forming the first and second numbers. A stored value designated as a product of second plurality of bits from the first number and a second plurality of bits from the second number is retrieved from a memory. The product is scaled with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number and the stored value is scaled with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number. A scaled product and a scaled stored value is summed to generate a value equivalent to a product of the first and second number, wherein the first number and the second number each have a number of bits equal to or greater than a total of the first and second plurality of bits.

Applicants submit that “generating a product by multiplying... using a digital signal processor (DSP)”, “retrieving a store value”, “scaling the product ... and scaling the stored value”, and “summing a scaled product and a scaled stored value to generate a value representing a product of the first and second numbers”, provide transformation or reduction of an article to a different state or thing. The first and second numbers have been transformed by virtue of the method of Claim 1 to a different, generated value representing the product. Thus, because the method of Claim 1 transforms an article to a different thing, Applicants believe that Claim 1 is directed to statutory subject matter under 35 U.S.C. § 101.

**Claims 1, 3, and 5-10 Produce a Useful, Tangible, and Concrete Result**

Furthermore, to meet the requirements of 35 U.S.C. § 101, “[t]he claimed invention as a whole must accomplish a practical application. That is, it must produce a ‘useful, concrete and tangible result.’” M.P.E.P. § 2106(II)(A) (quoting State Street Bank & Trust v. Signature Financial Group, Inc., 149 F.3d 1368, 1373, 47 USPQ2d 1596, 1601 (Fed. Cir. 1998)). State Street provides the following example of a claimed invention that produces a useful, concrete, and tangible result:

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[T]ransformation of data, representing discrete dollar amounts, by a machine through a series of mathematical calculations into a final share price, constitutes a practical application of a mathematical algorithm, formula, or calculation, because it produces 'a useful, concrete and tangible result' -- a final share price momentarily fixed for recording and reporting purposes and even accepted and relied upon by regulatory authorities and in subsequent trades.

State Street, 149 F.3d at 1373, 47 USPQ2d at 1601.

It is respectfully submitted that if "transformation of data...into a final share price" is statutory subject matter, as in the State Street case, then the method of Claim 1 is also statutory because it constitutes a practical application to produce a "useful, concrete, and tangible result", i.e., the value representing a product of the first and second number, wherein the first and second number each have a number of bits equal to or greater than the total of the first and second number of bits. By virtue of the method of Claim 1, the product of the two numbers can be obtained by the field programmable gate array despite the fact that the DSP of the array is capable of multiplying only a fewer number of bits than those forming the two numbers. As such, the result of the method clearly is "useful, concrete, and tangible" in that it is achieved without having to employ a DSP capable of multiplying at least the total number of bits of the two numbers.

For these reasons, Claim 1, as well as the claims dependent there from, are believed to clearly recite statutory subject matter.

**Claims 11-20 Transform an Article to a Different State**

Applicants also submit that the method of Claim 11 transforms and reduces articles to a different state or thing. Claim 11 recites a method for implementing a multiplier on a field programmable gate array. The method includes configuring a digital signal processor to perform multiplication on a first plurality of bits from a first number and a first plurality of bits from a

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second number. Products are stored resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number in a memory. An output from the DSP is routed to an adder such that the output from the DSP is scaled according to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number. An output of the memory is routed to the adder such that the output from the memory is scaled according to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number. A value representing a product of the first and second number is output where the first and second number each have more than the first plurality of bits, wherein the DSP is configured to support multiplication of no more than the first plurality of bits.

Applicants submit that "configuring a digital signal processor (DSP) to perform multiplication", "storing products resulting from multiplication", "routing an output from the DSP to an adder such that the output from the DSP is scaled", "routing an output of the memory to the adder such that the output from the memory is scaled", and "outputting a value..." provide transformation or reduction of an article to a different state or thing. The DSP, memory, routing from the DSP to adder, and routing from the memory to the adder on the field programmable gate array have clearly been transformed. Thus, because the method of Claim 11 transforms the components on the field programmable gate array to a different state, Applicants submit that Claim 11 is directed to statutory subject matter under 35 U.S.C. § 101. Furthermore, Applicants submit that the DSP, memory, routing from the DSP to adder, and routing from the memory to the adder on the field programmable gate array also transform the first number and second number to a value representing a product of the first and second numbers, despite the fact that the DSP is configured to support multiplication of no more than the first plurality of bits. Thus because the method of Claim 11 transforms the first and second numbers to a different state, Applicants submit that Claim 11 is directed to statutory subject matter under 35 U.S.C. § 101.

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**Claims 11-20 Produce a Useful, Tangible, and Concrete Result**

As stated above, in the State Street decision, the Court of Appeals for the Federal Circuit held that “transformation of data, representing discrete dollar amounts, by a machine through a series of mathematical calculations into a final share price constitutes a practical application ... ... because it produces ‘a useful, concrete, and tangible result’”. Applicants respectfully submit that the method of Claim 11 comprising, *inter alia*, outputting a value representing a product of a first and second number where the first and second number each have more than a first plurality of bits, but wherein a DSP is configured to support multiplication of no more than the first plurality of bits as described in Claim 11, similarly represent statutory subject matter under 35 U.S.C. § 101. That is, the configuring of a DSP, storing of products in a memory, routing of an output from the DSP to an adder, routing of an output from the memory to an adder, and outputting provide a “useful, concrete, and tangible result”, i.e., a value representing a product of a first and second number where the first and second number each have more than the first plurality of bits. The product of the two numbers is obtained by the field programmable gate array despite the fact that the DSP of the array is capable of supporting multiplication of no more than the first plurality of bits, and thus it is not necessary to employ a DSP capable of multiplying more than that number of bits.

For these reasons, Claim 11 as well as the claims dependent there from are believed to clearly recite statutory subject matter as well.

Claims 17-20 include subject matter similar to that of Claims 11-16 and therefore are submitted to be directed to patentable subject matter for the same reasons. Therefore, withdrawal of the rejections is respectfully requested.

Claims 1-7, 9, and 11-20 are rejected under 35 U.S.C. §102(e) and §103(a) as being unpatentable over Regis.

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It is submitted that Regis does not render claims 1, 3, 5-22 unpatentable under 35 U.S.C. §102(e) and §103(a).

Regis includes a disclosure of a multichannel filter for CDMA modems that permits multiple serial, digital bit streams to be filtered by digital signal processing techniques including sample weighting and summing functions. Each individual channel may have custom weighting coefficients or weighting coefficients common for all channels. If the weighting coefficients are by adaption, the same approach may be taken. The multichannel FIR filter is implemented with no multipliers and a reduction in the number of adders. To increase the speed of operation, the filter structure utilizes look-up tables storing the weighting coefficients. The invention can be embodied as either as a field programmable gate array or an application specific integrated circuit. The use of look-up tables saves significant chip resources (see Regis Abstract).

Applicants submit that Regis does not teach or suggest a method for performing multiplication on a field programmable gate array that includes generating a product by multiplying a first plurality of bits from a first number and a first plurality of bits from a second number using a digital signal processor (DSP) configured to perform multiplication on a fewer number of bits than those forming the first and second numbers, retrieving a stored value designated as a product of a second plurality of bits from the first number and a second plurality of bits from the second number from a memory, scaling the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number, and summing a scaled product and a scaled stored value to generate a value representing a product of the first number and the second number, wherein the first number and the second number each have a number of bits equal to or greater than a total of the first and second plurality of bits.

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The Office Action mailed 9/10/2007 states in part that

Re claim 1, Regis discloses in Figures 2, 4-5, and 8 a method for performing multiplication on a field programmable gate array (e.g. abstract and col. 1 lines 13-19 wherein the multiplication is performed in FIR filter; and general architecture is seen in Figure 4B), comprising:

generating a product (e.g.  $y_k$  as product of  $x$  inputs [ $x_k-x_{k-3}$ ] and  $c$  coefficients [ $c_0-c_3$ ] in Figure 2 and as FIR 0 in Figure 4B) multiplying a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. the first number is  $x$  input and second number is the corresponding coefficient as simply seen in FIR Figure 2);

retrieving a stored value designated as a product (e.g. by utilizing LUTs as seen in Figure 8A or 8B) of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. the first number is  $x$  input and second number is the corresponding coefficient as simply seen in FIR 1 in Figure 4B);

scaling (e.g. by multiplying with corresponding weights 37 in Figure 4B) the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number (e.g. multiplying w(0) 37 with product of FIR 0 as  $y(0)$ , by multiplier 24 in Figure 4B) and scaling (e.g. by multiplying with corresponding weights 37 in Figure 4B) the stored value with respect to a position of the second plurality of bits from the second number and a position of the second plurality of bits from the second number (e.g. multiplying w(1) 37 with product of FIR 1 as  $y(1)$ , by multiplier 24 in Figure 4B); and

summing a scaled product and a scaled stored value (e.g. by adder 46 in Figure 4B).

(9/10/2007 Office Action, pp. 4-5) (Emphasis Added).

Firstly, the Office points to FIR 1 in Figure 4B as support that Regis discloses retrieving a stored value designated as a product of a second plurality of bits from the first number and a second plurality of bits from the second number (9/10/2007 Office Action, p. 4).

On the contrary, Applicants submit that the FIR filter (FIR 1) 20 in Figure 4B generates a signal  $y_k$  by multiplying an input signal with  $x_k$  with a filter coefficient weights  $c_i$  and summing the products (see Regis column 4, lines 27-42 and Figure 1). The FIR 1 in Figure 4B is not a

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memory and the FIR 1 in Figure 4B does not store a value designated as a product of a second plurality of bits from a first number and a second plurality of bits from a second number.

Furthermore, the Office acknowledges that “multiplication is performed in [the] FIR filter” and even refers to FIR 0 in Figure 4B as support to illustrate that Regis generates a product by multiplying a first plurality of bits from a first number and a first plurality of bits from a second number (9/10/2007 Office Action, p. 4).

The Office appears to alternatively suggest that a look up table (LUT) 56 illustrated in Figures 8A and 8B provides support that Regis discloses “retrieving a stored value designated as a product”. Applicants submit, however, that in an embodiment where a LUT is used in Regis, all values are precomputed and stored in the memory array (see Regis Figure 8A and 8B and column 6, lines 48-51). No circuitry, exists to generate a product by multiplying a first plurality of bits from a first number and a first plurality of bits from a second number using a digital signal processor. When a LUT is implemented, no FIR filters are implemented (see Regis Figure 8B and column 6, lines 28-54).

Secondly, the Office points to multipliers 24 and weights 37 as support that Regis discloses scaling the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number (9/10/2007 Office Action, pp. 4-5).

On the contrary, the weighting coefficients 37 disclosed in Regis are applied to individually filtered signals for power control, equalizing the power of gain between individual channels (see Regis column 5, lines 42-46, and Figure 4B). The weighting coefficients 37 are not used to scale a product of a first plurality of bits from a first number and a first plurality of bits from a second number with respect to a position of the first plurality of bits, nor are the weighting

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coefficients 37 used to scale a stored value with respect to a position of the second plurality of bits.

In contrast, claim 1, as amended, states

A method for performing multiplication on a field programmable gate array, comprising:

generating a product by multiplying a first plurality of bits from a first number and a first plurality of bits from a second number using a digital signal processor (DSP) configured to perform multiplication on a fewer number of bits than those forming the first and second numbers;

retrieving a stored value designated as a product of a second plurality of bits from the first number and a second plurality of bits from the second number from a memory;

scaling the product with respect to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number; and

summing a scaled product and a scaled stored value to generate a value representing a product of the first number and the second number, wherein the first number and the second number each have a number of bits equal to or greater than a total of the first and second plurality of bits.

(Claim 1, as Amended) (Emphasis Added).

Claims 11, 17, and new claims 21 and 22 include similar limitations.

Given that claims 3, and 5-10 depend from claim 1, claims 12-16 depend from claim 11, and claims 18-20 depend from claim 17; it is likewise submitted that claims 3, 5-10, 12-16, and 18-20 are also patentable under 35 U.S.C. §102(e) and §103(a) over Regis.

In view of the arguments set forth herein, it is respectfully submitted that the applicable rejections have been overcome. Accordingly, it is respectfully submitted that claims 1, 3, 5-22 should be found to be in condition for allowance.

The Examiner is invited to telephone Applicant's attorney (217-377-2500) to facilitate prosecution of this application.

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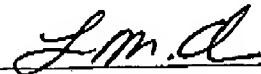
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If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

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